2nd International Symposium on Master Engineering
Booklets

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Title: Design and implementation of the debugging and scheduling logic section for a RISCV

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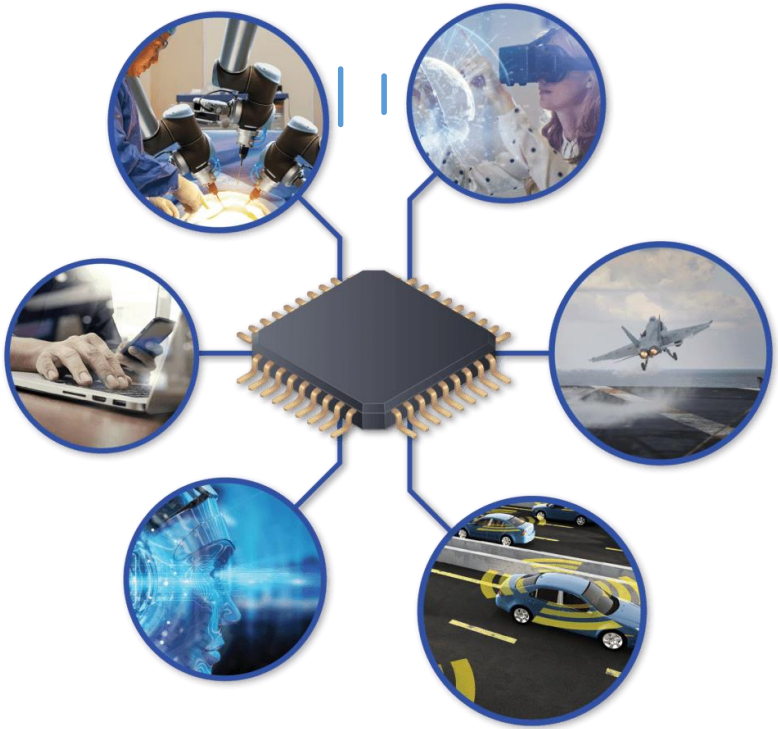
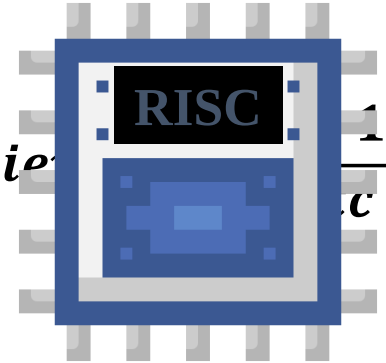
Introducción



Introducción



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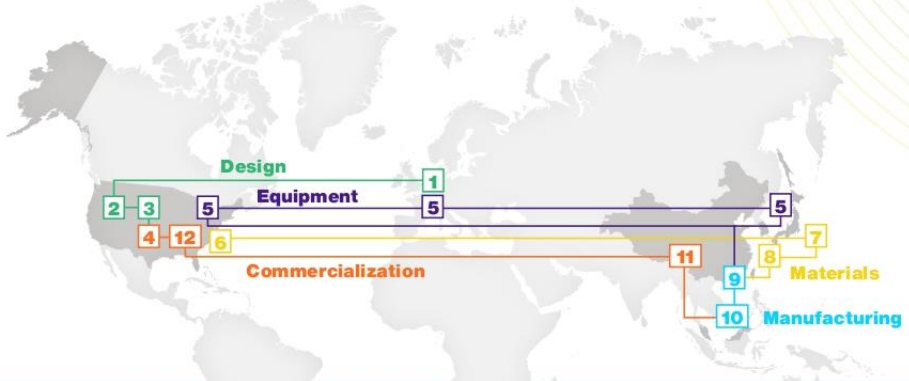
$$Eficie \quad \frac{1}{c * nc)}$$

Instrucción

Ejecución

The semiconductor value chain is truly global and relies on the specialized capabilities of different geographic areas



Illustrative: The global journey of a smartphone application processor

Design

1 A **European** firm licenses IP on application processor architecture

2 A **US** EDA firm provides highly sophisticated software for chip design

3 A **US** fabless firm designs (and commercializes) the chip

Commercialization

4 The chip is selected ("designed in") by a **US** smartphone OEM to power its new device

Equipment

5 Highly advanced manufacturing equipment is developed by companies in the **US**, **Japan** and **Europe**, leveraging decades of global R&D efforts

Manufacturing

9 A foundry in **Taiwan** Imprints the wafers with an array of integrated circuits; "patterned" wafers are stacked and interconnected

10 Individual chips are separated and packaged by an OSAT in **Malaysia**

11 The chip is shipped to the smartphone OEM's assembly partner in **China**, who incorporates it into a circuit board inside the phone

Materials

6 Silicon dioxide is mined in the **US** and refined into metallurgical grade silicon

7 The silicon is melted and re-crystallized to form a large single crystal called an ingot by a polysilicon manufacturer in **Japan**

8 The ingot is sliced into several wafers in **South Korea**, which are then polished and shipped to a fabrication plant

12 The smartphone is sold to a consumer in the **US**

ANTECEDENTES

Beijing, China

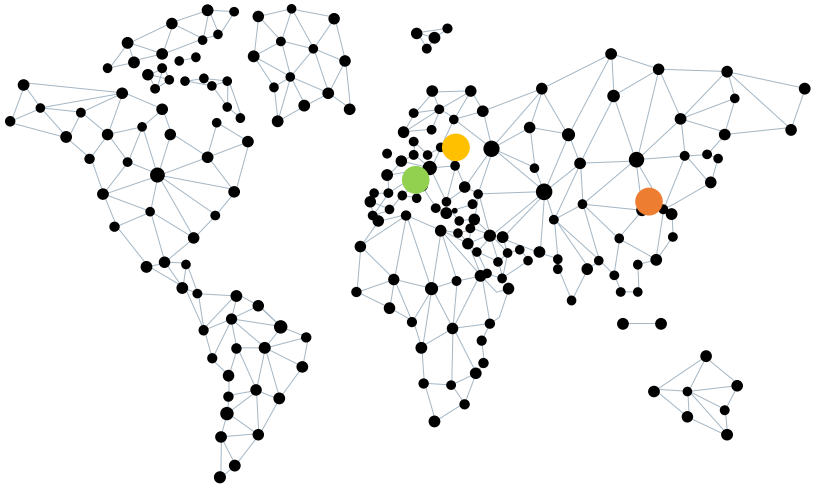
- A fast on-chip debugging design for RISC-V processor
- A novel method for on-chip debugging based on RISC-V processor

Warsaw, Poland

Serial Wire Debug Open Framework for Low–Level Embedded Systems Access

Seúl, Corea

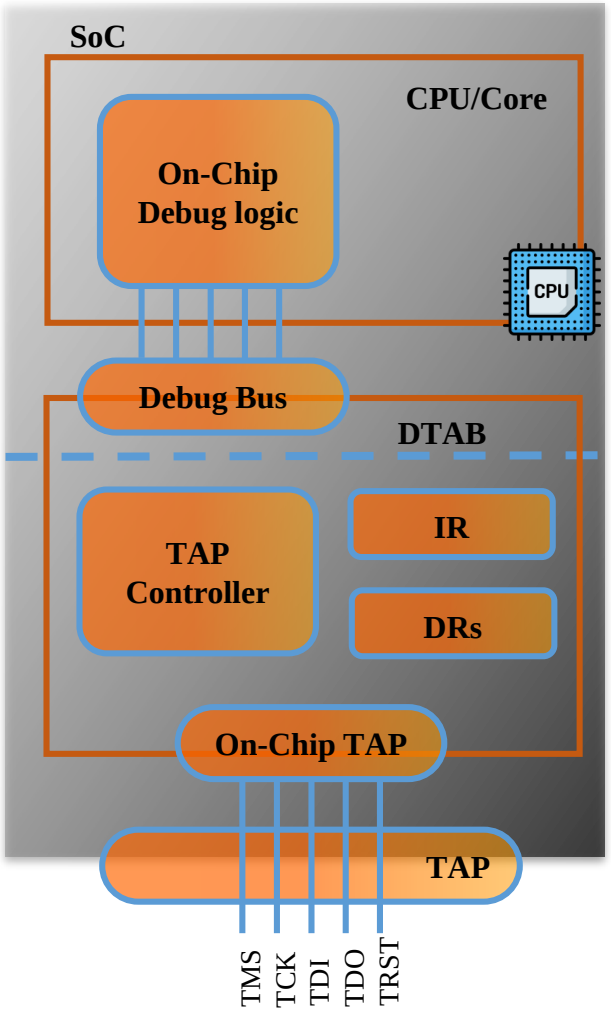
Reusable Embedded Debugger for 32bit RISC Processor Using the JTAG Boundary Scan Architecture



Objetivo general

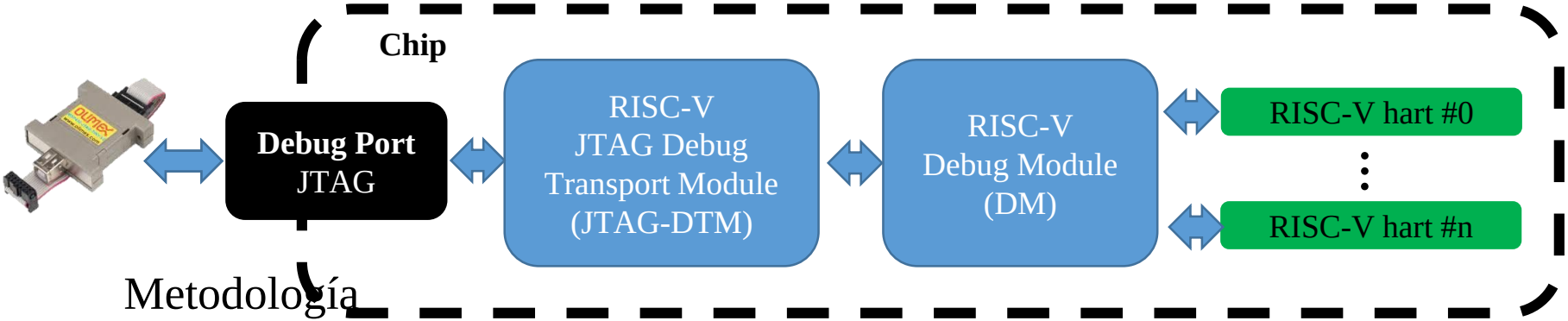
Diseñar e implementar la unidad lógica de depuración y programación para un procesador RISCV.

JTAG



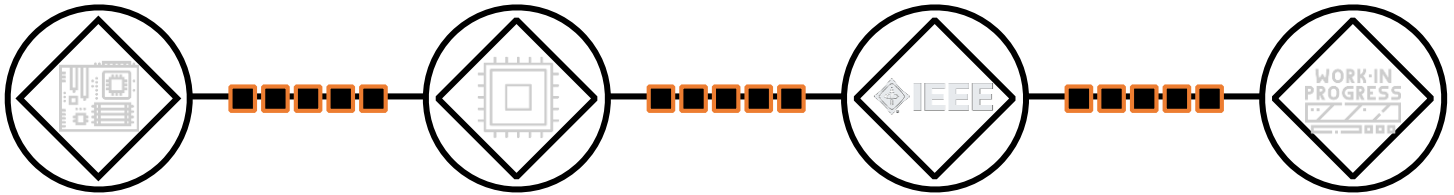
Estándar JTAG

Permite el control total del sistema objetivo a nivel de hardware.



Metodología

Metodología

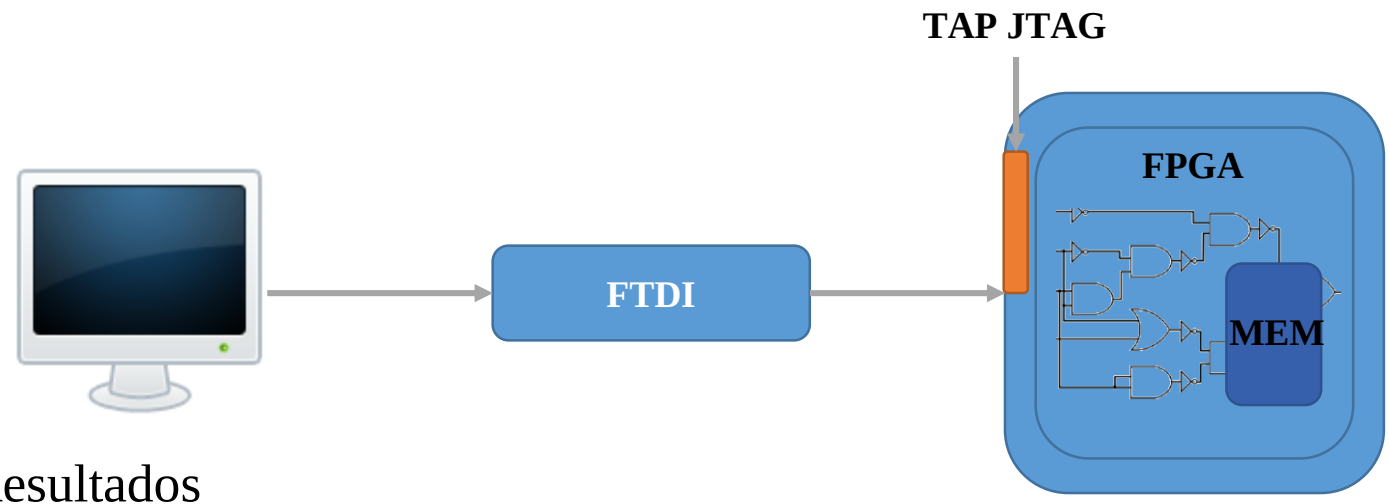


Arquitectura de computadoras

RISC-V

JTAG

Módulo de depuración



Resultados

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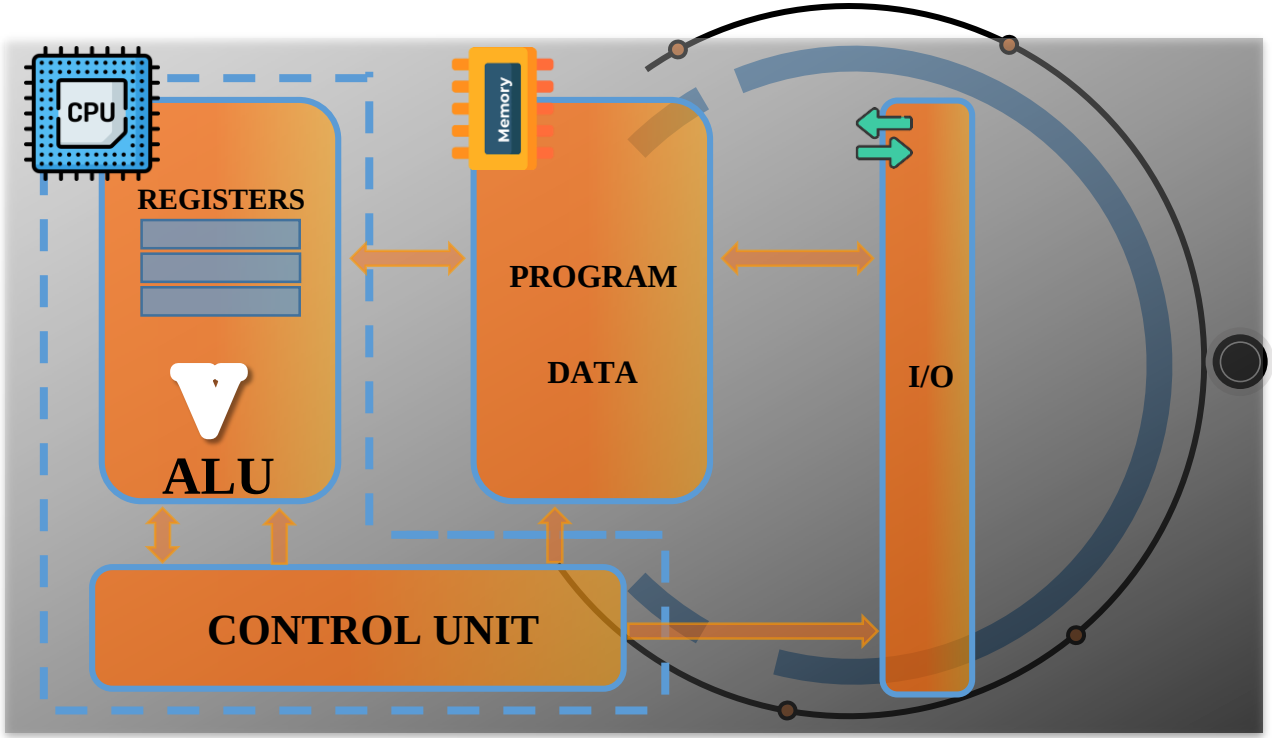
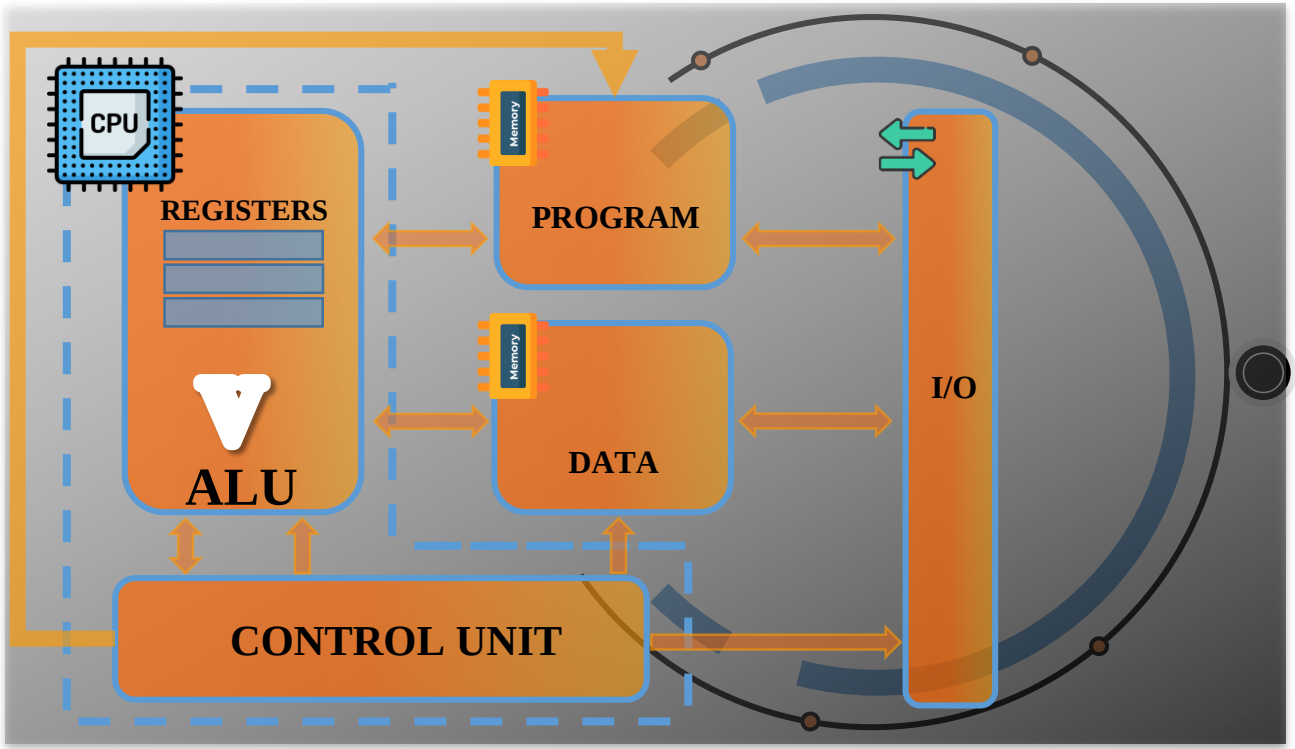
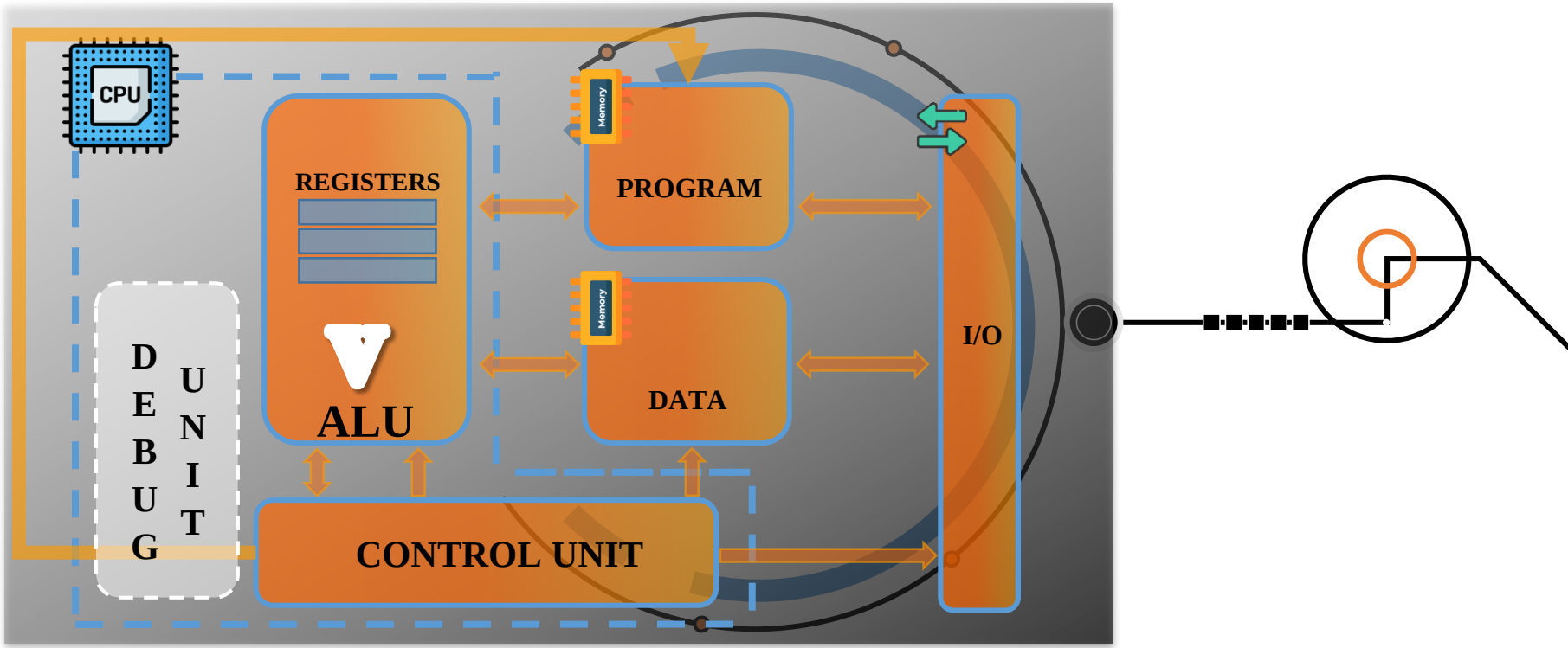
Von Neumann



Harvard


CPU
REGISTERS
ALU
Memory
PROGRAM
Memory
DATA
I/O
CONTROL UNIT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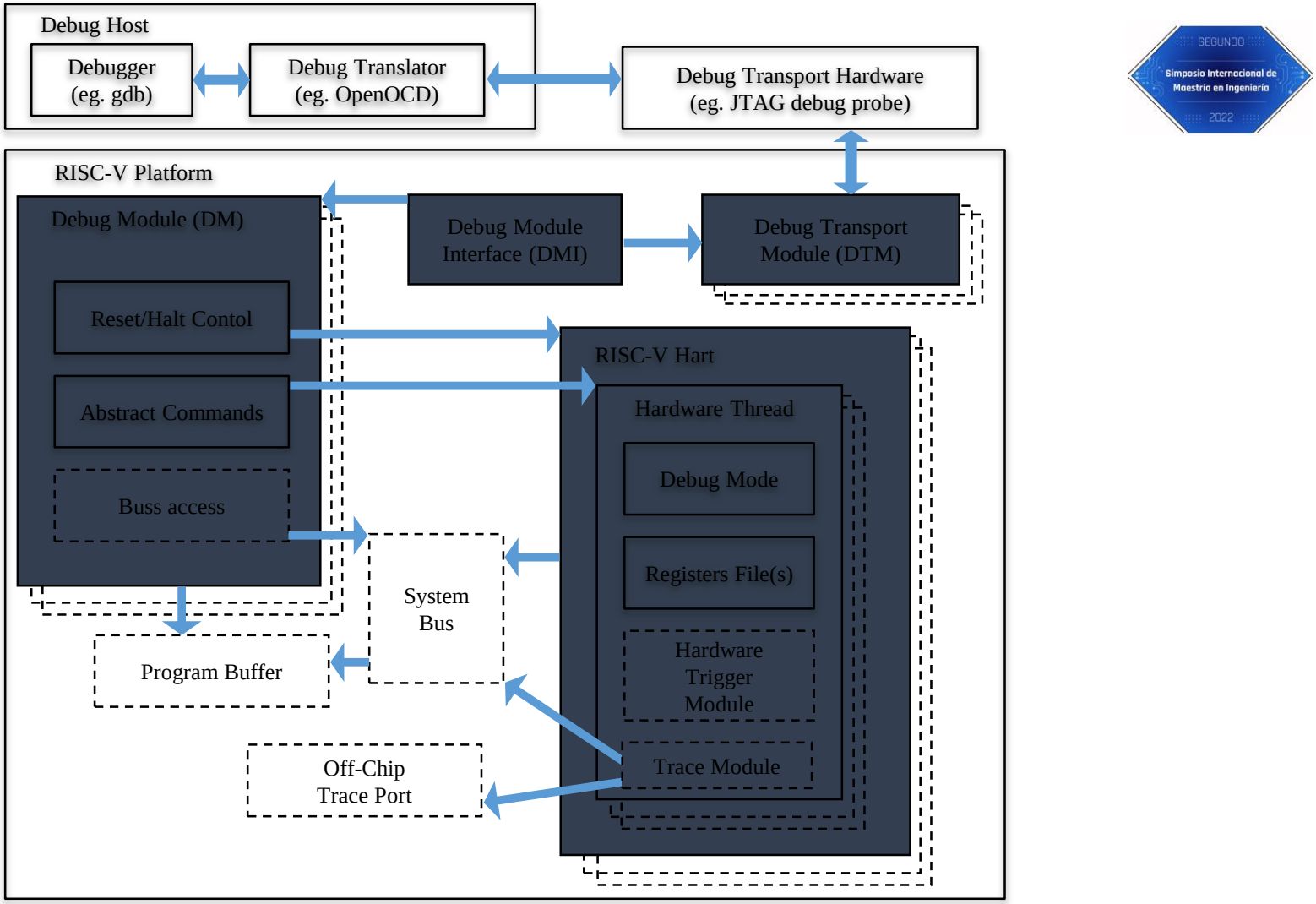
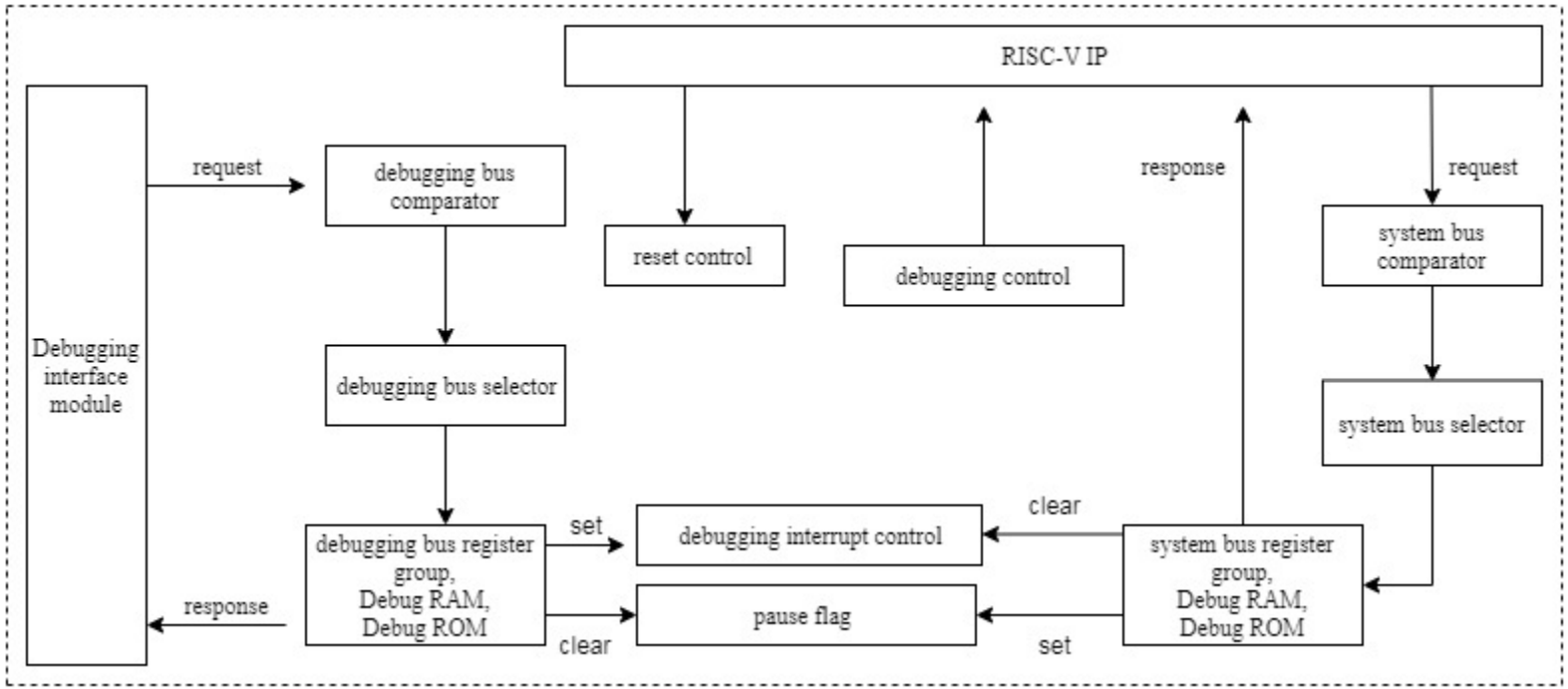
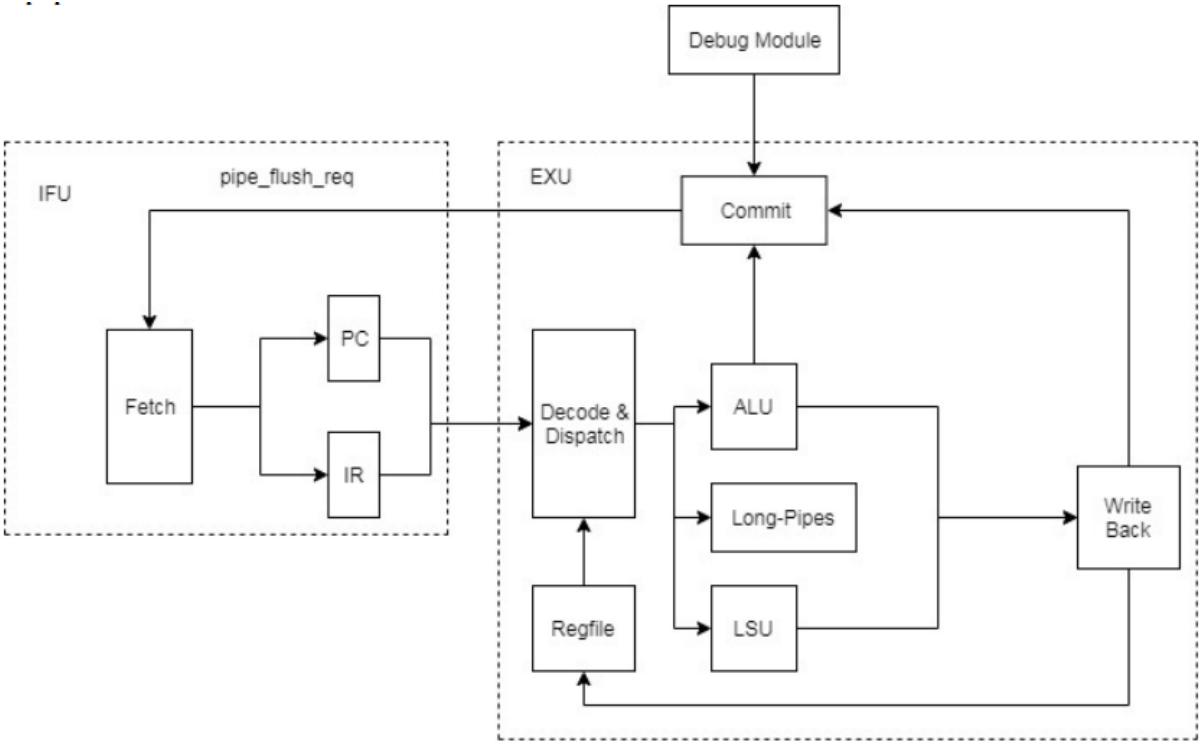

Debug Host
Debugger
(eg. gdb)
Debug Translator
(eg. OpenOCD)
Debug Transport Hardware
(eg. JTAG debug probe)
RISC-V Platform
Debug Module (DM)
Reset/Halt Contol
Abstract Commands
Buss access
Debug Module
Interface (DMI)
Debug Transport
Module (DTM)
RISC-V Hart
Hardware Thread
Debug Mode
Registers File(s)
Hardware
Trigger
Module
Trace Module
System
Bus
Program Buffer
Off-Chip
Trace Port

A fast on-chip debugging design for RISC-V processor



A novel method for on-chip debugging based on RISC-V processor



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